28. 05. 2004

Sertifikaat

REPUBLIEK VAN SUID AFRIKA

PATENT KANTOOR
DdepartEMENT VAN HANDEL EN NYWERHEID

Certificate

REPUBLIC OF SOUTH AFRICA

PATENT OFFICE
DEPARTMENT OF TRADE AND INDUSTRY

Hiermee word gesertifiseer dat
This is to certify that

EP04/03666

the documents annexed hereto are true copies of:

Application forms P.1 and P.2, provisional specification and drawings of South African Patent Application No. 2003/2684 as originally filed in the Republic of South Africa on 7 April 2003 in the name of SUNTKEN ARTUR WILHELM for an invention entitled:" DIGITAL SENSOR ".

Geteken te **PRETORIA** in die Republiek van Suid-Afrika, hierdie 4th dag van **April 2004**
Signed at **PRETORIA** in the Republic of South Africa, this 4th day of **April 2004**

.....
Registrar of Patents

EPUBLIC OF SOUTH AFRICA

FORM P2
PATENTS ACT, 1978

REGISTER OF PATENTS

FFICIAL APPLICATION NO.	LODGING DATE: PROVISIONAL	ACCEPTANCE DATE
1 01 2003/2684	22 7 Apr 2003	47
ITERNATIONAL CLASSIFICATION	LODGING DATE: COMPLETE	GRANTED DATE
1	23	
ITERNATIONAL APPLICATION NO.	LODGING DATE: INTERNATIONAL	

JLL NAME(S) OF APPLICANT(S)/PATENTEE(S)

1

SUNTKEN, Artur, Wilhelm

PLICANTS SUBSTITUTED:	DATE REGISTERED

SIGNEE(S)	DATE REGISTERED

ILL NAME(S) OF INVENTOR(S)

1

SUNTKEN, Artur, Wilhelm

IORITY CLAIMED	COUNTRY	NUMBER	DATE
3 - Use International abbreviation for country e Schedule 4)	33	31	32

LE OF INVENTION

1

DIGITAL SENSOR

DDRESS OF APPLICANT(S)/PATENTEE(S)

554 WITOGIE STREET, THE WILLOWS, PRETORIA, RSA

DDRESS FOR SERVICE	REF
1 **HAHN & HAHN INC, PRETORIA**	
TENT OF ADDITION NO.	DATE OF ANY CHANGE
ESH APPLICATION BASED ON	DATE OF ANY CHANGE

REPUBLIC OF SOUTH AFRICA

REPUBLIC OF SOUTH AFRICA
PATENTS ACT, 1978

FORM P1

APPLICATION FOR A PATENT AND ACKNOWLEDGEMENT OF RECEIPT

[Section 30 (1) - Regulation 22]

Revenue stamps or revenue franking machine impression

Official date stamp

The grant of a patent is hereby requested by the undermentioned applicant on the basis of the present application filed in duplicate

OFFICIAL APPLICATION NO.
21 01 2003/2684

(i) APPLICANT'S OR AGENT'S REFERENCE

(ii) FULL NAME(S) OF APPLICANT(S)
71 **SUNTKEN, Artur, Wilhelm**

(iii) ADDRESS(ES) OF APPLICANT(S)
554 WITOGIE STREET, THE WILLOWS, PRETORIA, RSA

(iv) TITLE OF INVENTION
54 **DIGITAL SENSOR**

(v) The applicant claims priority as set out on the accompanying form P2.
The earliest priority claimed is Country: Number: Date:

(vi) This application is for a patent of addition to Patent Application No. 21 01

(vii) This application is a fresh application in terms of section 37 and is based on Patent Application No. 21 01

(viii) This application is accompanied by:

X	1.	A single copy of a provisional specification of 6 pages.
X	2.	Drawings of 4 sheets
	3.	Publication particulars and abstract (form P8 in duplicate).
	4.	A copy of Figure __ of the drawings for the abstract.
	5.	An assignment of invention.
	6.	Certified priority document(s) (state number):
	7.	Translation of the priority document(s).
	8.	An assignment of priority rights.
	9.	A copy of the form P2 and the specification of SA Patent Application No. 21 01
X	10.	A declaration and power of attorney form P3.
	11.	Request for ante-dating on form P4.
	12.	Request for classification on form P9.
	13.	In terms of section 31(1) the applicant has added additional revenue stamps to this form for claiming priority after 12 months but before 15 months from the priority filing date.
X	14.	Form P2 + copy

(ix) 74 Address for service: **HAHN & HAHN INC, 222 Richard Street, HATFIELD, 0083, Pretoria**

Dated this 7 day of April 2003

Signature of applicant(s) or agent

This duplicate will be returned to the applicant's address for service as proof of lodging but is not valid unless endorsed with an official stamp

Received
REGISTRAR OF PATENTS DESIGNS, TRADE MARKS AND COPYRIGHT
Official date stamp
2003 -04- 07
Registrar of Patents

REGISTRATEUR VAN PATENTE MODELLE HANDELSMERKE EN OUTEURSREG

HAHN & HAHN INC.

FORM P6

REPUBLIC OF SOUTH AFRICA
PATENTS ACT, 1978

PROVISIONAL SPECIFICATION

[Section 30(1) - Regulation 27]

OFFICIAL APPLICATION NO	
21	01 *2003/2684

LODGING DATE	
22	7 Apr 2003

FULL NAME(S) OF APPLICANT(S)	
71	SUNTKEN, Artur, Wilhelm

FULL NAME(S) OF INVENTOR(S)	
72	SUNTKEN, Artur, Wilhelm

TITLE OF INVENTION	
54	DIGITAL SENSOR

DIGITAL SENSOR

FIELD OF THE INVENTION

This invention relates, in general, to the field of digital sensors and, in particular, to the field of digital passive infra-red (PIR) sensors.

BACKGROUND TO THE INVENTION

Passive infra-red (PIR) sensors are typically, but not exclusively, used to detect the presence of humans in a particular zone. PIR sensors find ready application in the fields of sensor lights, intruder detectors, and occupation detectors (used, for example, to switch and/or regulate lighting and/or air-conditioning systems in hotels, offices, and the like so as to conserve energy).

The Inventor is aware of conventional PIR sensors which typically include a conventional analogue PIR element connected, via a capacitive node having a high impedance, to an impedance converter for converting the high impedance to a relatively low impedance on the output of the sensor without amplification. Accordingly, an analogue signal is available at the output of the conventional PIR sensor.

SUMMARY OF THE INVENTION

According to the invention there is provided a digital sensor which includes

an analogue passive infra-red (PIR) element; and

an analogue to digital converter (ADC) connected to the output of the analogue PIR element so as to provide a digital output.

The PIR element is typically a conventional PIR element.

The ADC may include an input amplifier.

The ADC may include an input means configured to interface with the PIR element.

The sensor may include a decimation filter connected to an output of the ADC for filtering out unwanted high frequency components of the output of the ADC and providing a high resolution output.

The digital sensor may include a serial interface for converting a parallel output of the decimation filter to a serial output. This allows the output of the digital sensor to be available on a single pin.

The digital sensor typically includes control means for controlling the operation of the ADC, the decimation filter, and the serial interface.

The ADC, the decimation filter, the serial interface, and/or the control means are typically provided as an integrated circuit (IC).

The digital sensor is typically housed within a housing so that it can be used for direct connection to an external processor in a system incorporating the digital sensor.

DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described, by way of non-limiting example, with reference to the accompanying drawings wherein:

Figure 1 shows, schematically, a block diagram of a conventional analogue passive infra-red (PIR) sensor;

Figure 2 shows, schematically, a block diagram of a digital sensor, in accordance with the invention;

Figure 3 shows, schematically, a more detailed block diagram of the analogue to digital converter (ADC) shown in Figure 2; and

Figure 4 shows, schematically, a PIR element connected to an integrated circuit (IC) including the rest of the features of the digital sensor.

In Figure 1 reference numeral 10 generally indicates a conventional analogue passive infra-red (PIR) sensor. The conventional sensor 10 includes a a conventional analogue PIR element 12 connected, via a capacitive node 14 having a high impedance, to an impedance converter 16 for converting the high impedance to a relatively low impedance on the output of the conventional sensor 10 without amplification. Accordingly, an analogue signal is available at the output of the conventional sensor 10.

In Figures 2 and 4 reference numeral 20 generally indicates a digital sensor in accordance with the invention. The digital sensor 20 includes a conventional analogue passive infra-red (PIR) element 12 and an analogue to digital converter (ADC) 22 connected to the output of the analogue PIR element 12 so as to provide a digital output. The ADC 22 typically also includes an input amplifier.

As shown in Figure 3, in particular, the ADC 22 includes an input means configured to interface with the PIR element 12. Accordingly, the ADC 22 includes an integrator 24 which feeds in series into a comparator 26 which in turn feeds in series into a digital feedback means 28. The output of the digital feedback means 28 is fed back via a digital to analogue converter (DAC) 30 and the appropriate interfacing circuitry (not shown) into a summing node 32 together with the output of the PIR element 12. In this example, the PIR element 12 behaves like a piezo element and typically has a capacitance of approximately 20 pF to 60 pF. The output of the DAC 30 is also capacitive. The output of the summing node 32 is fed into the integrator 24 to complete the circuit.

In use, the ADC 22 operates by attempting to maintain the input of the integrator 24 at an average of zero by the digital feedback means 28 via the DAC 30 so as to compensate (neutralise) the output of the PIR element 12. The digital feedback means employs a special algorithm to achieve overall stability of this configuration.

The digital output of the digital feedback means 28 (which is in fact the digital output of the ADC 22) is fed into a decimation filter 34 for filtering out unwanted high frequency components and providing a high resolution output. In this example, the decimation filter 34 generates a 16 bit digital signal with a sampling rate of approximately 1 kHz. The bandwidth of this signal is limited to frequencies below 20 Hz.

The amplitude value of the output of the decimation filter 34 is then fed into a serial interface 36 for conversion into a serial output. This allows the output of the digital sensor 20 to be available on a single pin. The serial interface 36 also operates as a data latch.

The digital sensor 20 typically includes control means 38 for controlling the operation of the ADC 22, the decimation filter 34, and the serial interface 36. An oscillator 40 is connected to the control means 38 to provide a clock. The ADC 22, the decimation filter 34, the serial interface 36, and the oscillator 40 are typically provided as an integrated circuit (IC) 42, as shown in particular in Figure 4, and the entire digital sensor 20 is housed within a housing (not shown) so that it can be used for direct connection to an external processor (not shown) in a system incorporating the digital sensor 20 in a simple and user-friendly manner.

In this example, the serial interface 36 is in the form of a one bit serial interface which places very little load on the external processor and, accordingly, allows for multiple digital sensors 20 to be controlled by a single low speed external processor in a system. The external processor determines the frequency at which the data is read and, due to the low cut-off frequency and the order of the decimation filter, the external processor can read the data at rates as low as 100 Hz. A data bit is sampled after a 0 – 1 – high impedance sequence generated by the external processor.

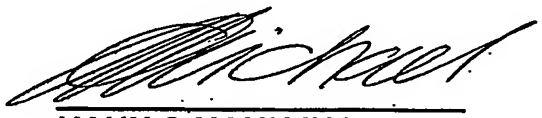
It is to be appreciated that the invention is not limited to the precise constructional details as described above and shown in the drawings as other

variations incorporating the gist of the invention are possible and fall within the scope of the invention.

The Inventor believes that this invention has the advantage that an external digital signal processor of a system incorporating one or more digital sensors according to the invention can be connected directly to such digital sensor obviating the need to develop any analogue signal processing or any analogue to digital conversion.

Furthermore, the digital sensor does not require a very clean supply voltage VDD and is inherently protected against radio frequency (RF) disturbances. The additional cost of providing a digital sensor compared to that of a conventional analogue sensor is relatively small. Accordingly, multi-sensor applications are very cost effective.

DATED THIS 7TH DAY OF APRIL 2003.



HAHN & HAHN INC.
AGENT FOR APPLICANT

SUNIKEN, Artur, Wilhelm

e2003/2684

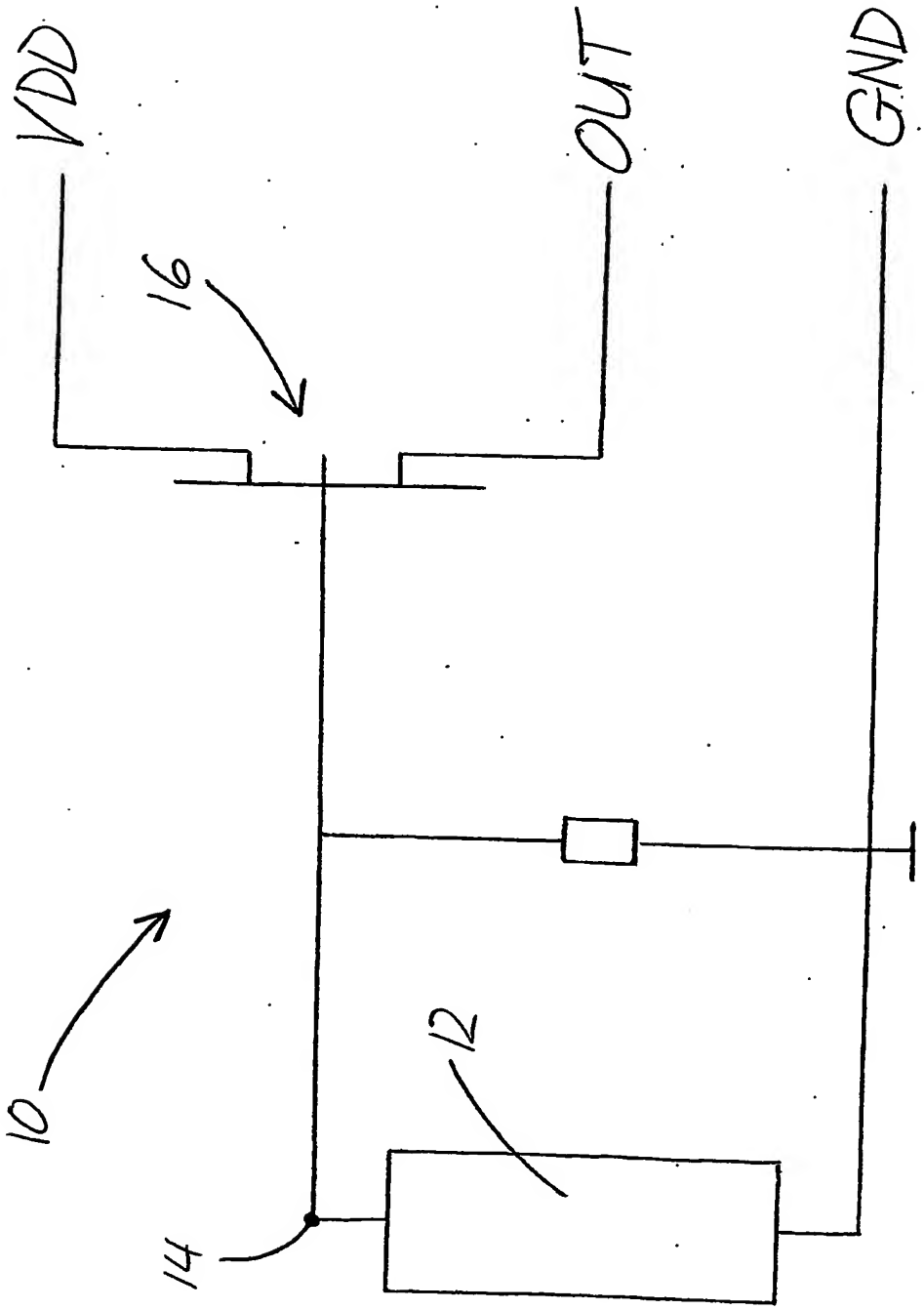


Figure 1

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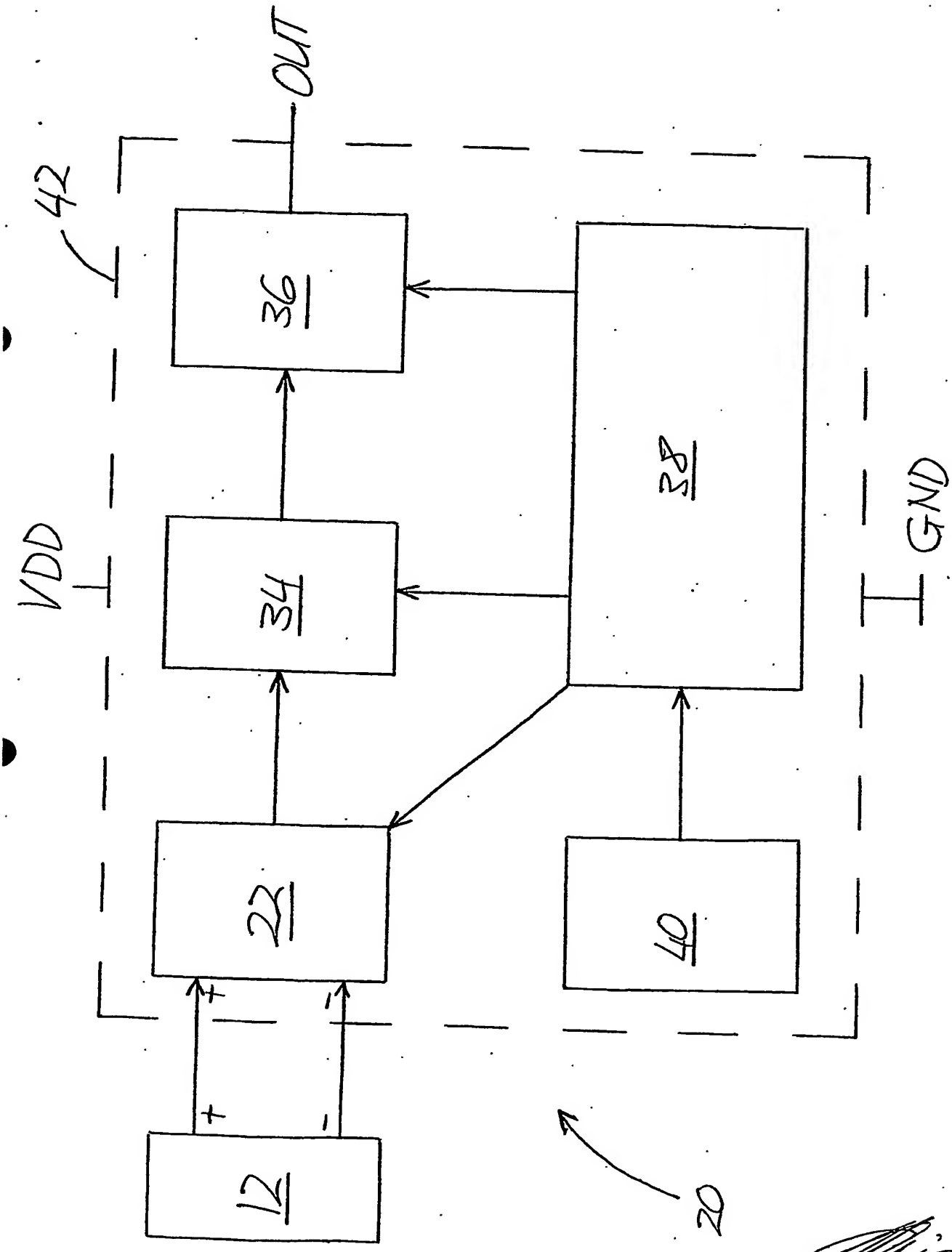

Figure 2

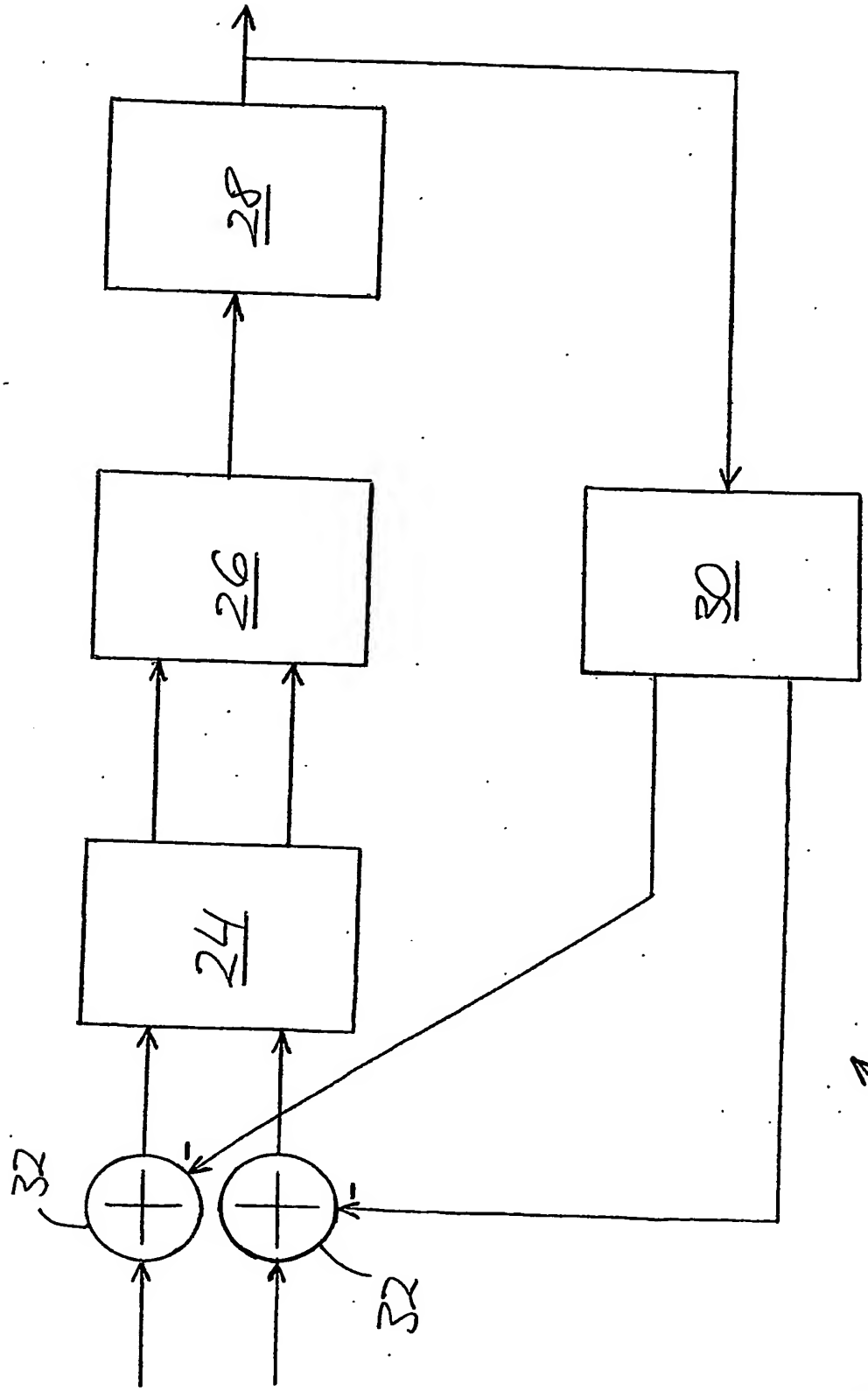

Figure 3

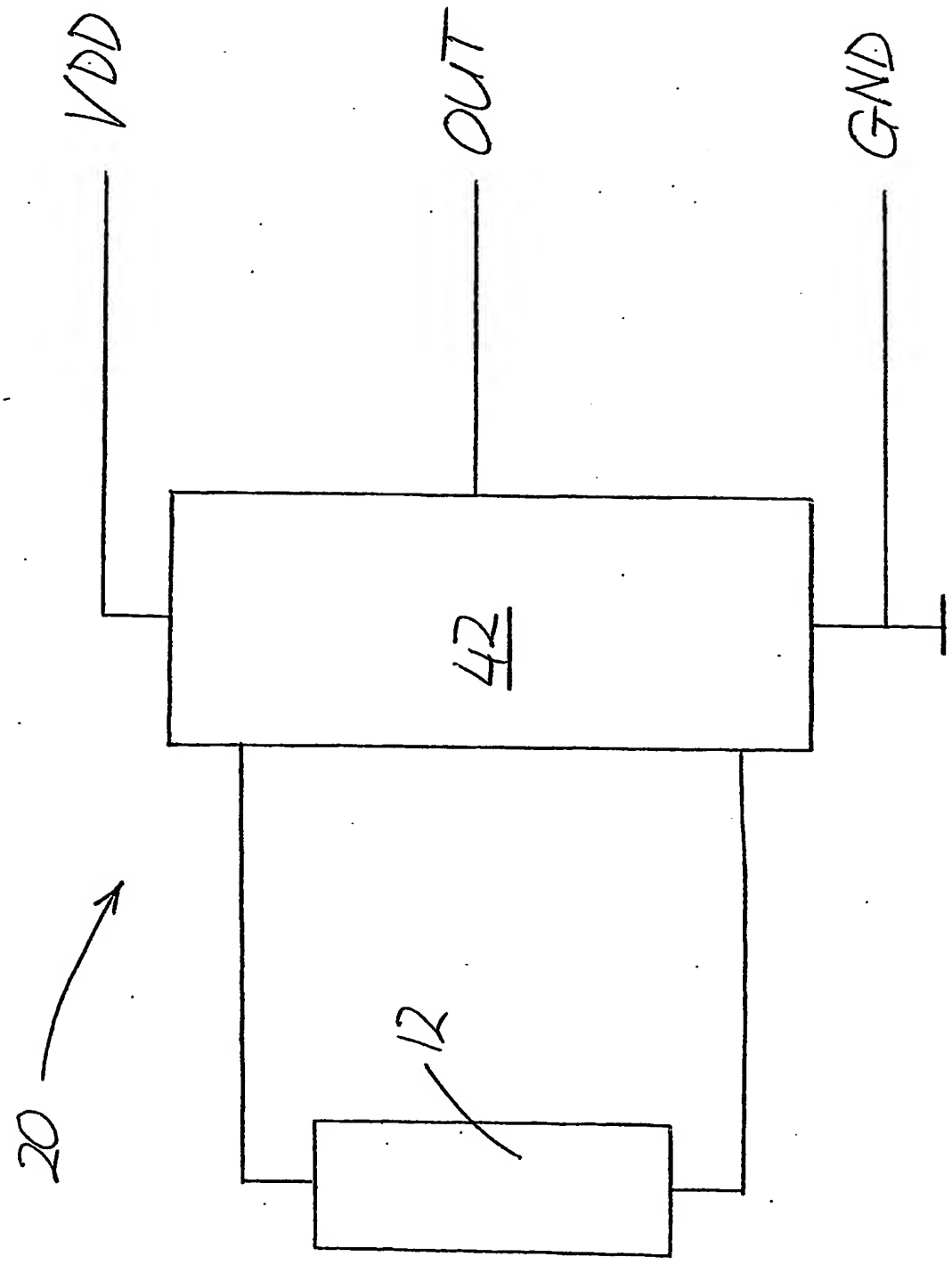

Figure 4